## IN THE SPECIFICATION

Please amend the specification as follows:

Please replace the paragraph beginning at page 7, line 26 with the following replacement paragraph:

Figures 3 through 8 are sectional views of the substrate 200 and various layers 208, 210, 212 and 214. Additionally, mask layers, etchings, and selective removals of residues and mask layers are also shown in Figures 3 and 8. In Figure 3, a first mask layer 300 is provided over the covering layer 216. In an embodiment, the first mask layer 300 includes at least one of titanium nitride (TiN), titanium (Ti), or silicon nitride (SiN). In another embodiment, the first mask layer 300 is deposited over the covering layer 216 by a spinning process. As shown in the sectional view of Figure 4, a second make layer 400 is disposed over the first mask layer 300. In one embodiment, the second mask layer 400 is applied in a similar manner as the first mask layer 300 (e.g. by spinning). In an embodiment, the second mask layer 400 includes a dielectric anti-reflective coating (DARC). In another embodiment, the second mask layer 400 includes silicon oxides. In this embodiment, the second mask layer 400 is patterned with a positive photoresist applied over the second mask layer. The photoresist is exposed to a known light wavelength for a set amount of time to define a pattern around the desired MRAM bit, thereby photosolubilizing the surrounding photoresist. The photosolubilized resist is subsequently removed in a developing step with, for example, a solution of tetramethyl ammonium hydroxide. The insoluble photoresist defined in the MRAM pattern remains and is used to pattern the second mask layer in an etching step (described herein).